

REMARKS

Claims 5 and 7 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The Examiner has objected to the “lower” claim language. Applicants present an amendment to claims 5 and 7 to address this issue. “Lower” appears to be a translation error from the original Italian application text and should instead read “shorter.”

Claims 4, 8 and 22-24 were rejected under 35 U.S.C. 102(e) as being anticipated by Hirose.

In claim 4, Applicants claim “reading, by the receiver block, of the data signal with a *different sampling period than the transmission period* of the transmitter block” (emphasis added) The Examiner asserts that this feature is taught by Hirose because block A and block B operate with different *clock signals*. The Examiner fails to provide any citation support for this assertion. Applicants request that the Examiner provide column and line number support for the assertion that Hirose blocks A and B operate with different clock signals. Applicants have reviewed columns 1 and 2 of Hirose which discuss Figure 1A and cannot find any teaching for the use of different clock signals for blocks A and B as asserted by the Examiner. In fact, there are no clock signals illustrated at all in Figure 1A.

Nonetheless, the issue of different *clock signals* is not relevant to the claim limitation of *different periods*. The claim limitation at issue concerns having the reading operation occur with a sampling period that is different from the transmission period. The Examiner’s citation to “clock signals” does not anticipate the claimed different read sampling period and transmit period requirement of claim 4. Applicants accordingly submit that the Examiner has failed to meet each claim limitation with the teachings of the Hirose reference.

In view of the foregoing, allowance of claim 4 is requested.

In claim 8, Applicants claim, in the context of “a first *bi-directional line*,” the “generating, on a couple of further lines, a couple of unidirectional signals indicating the transmission direction on the first bi-directional line between said first block and said second block, a *negotiation to define the transmission direction* being controlled by a further transmission request signal driven by the second block” (emphasis added). The Examiner asserts that this feature is taught by Hirose Figures 2A-2C. The Examiner further points to the counters

18 and 18A. Applicants disagree with the Examiner's technical analysis in application to the claim language.

The counters 18 and 18A of Hirose function to count stages (or commands) and thus ensure that there is not a transmission of more stages than the receiver can simultaneously process (see, col. 4, lines 15-64). This issue of trying to prevent congestion at the receiver has nothing to do with "a negotiation to define the transmission direction" as claimed. The Examiner's citation to Hirose fails to identify any manner with which Hirose functions to make a transmission direction negotiation. The limited teaching provided by the counters 18 and 18A is to prevent overloading transmission of information in a single direction, not a negotiation as to which direction between two blocks the transmission is to take.

In view of the foregoing, allowance of claim 8 is requested.

In claim 22, Applicants claim that "the first, second and third communication lines are *bi-directional*." The Examiner points to Hirose Figures 1A and 2C. Applicants fail to see the pertinence of these Hirose figures to the claim bi-directional communication lines. These figures clearly use a single-headed arrow for each communication line. Those skilled in the art understand this single-headed arrow to mean and refer to a *unidirectional* communication line.

Applicants further claim "control signals" specifying for the bi-directional communications line "which of the first and second communication blocks is a transmitter of the data signal and which of the first and second communication blocks is a receiver of the data signal." In a bi-directional communication line architecture this control over transmitter and receiver functionality is important since it defines which of the two directions on the line is active. The Examiner again points to the counters 18 and 18A. However, the counters 18 and 18A of Hirose function to count stages (or commands) and thus ensure that there is not a transmission of more stages than the receiver can simultaneously process (see, col. 4, lines 15-64). This issue of trying to prevent congestion at the receiver has nothing to do with controlling which block is going to be the transmitter and which block is going to be the receiver when those blocks are connected by a bi-directional communication line as claimed. The Examiner's citation to Hirose fails to identify any manner with which Hirose functions to control

transmission direction, and transmitter/receiver identification, in a bi-directional communication line system.

In view of the foregoing, allowance of claim 22 is requested.

With respect to claim 24, Applicants cancel the claim thus rendering the rejection moot.

Claims 2-3, 14-17 and 25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose in view of Dabral.

Turning first to claim 2, Applicants claim "said synchro signal is delayed for communication over the third line with respect to the data signal which is communicated over the first line." The Examiner correctly concedes that this is not taught by Hirose. Dabral teaches delaying a strobe signal to allow data to be set. However, this delayed strobe signal is not being delayed with respect to the communication of data from the sending domain (transmitter block) to the receiving domain (receiver block). The Dabral strobe signal simply controls the operation of latches 13/14 within a block or domain. This delayed strobe signal in Dabral is not a delayed synchro signal communicated as is claimed by Applicants between blocks over the third line in a delayed manner with respect to a data signal communicated over the first line. Dabral fails to teach a relationship between the strobe and data in terms of communications lines used, the included transmit and receive blocks, and the effect achieved, as is claimed by Applicants.

In view of the foregoing, allowance of claim 2 is requested. Claims 14 and 25 are asserted to be patentable over Hirose and Dabral for at least the same reasons as claim 2.

Claims 6, 9, 10, 19 and 21 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose in view of the admitted prior art.

In claim 6, Applicants claim "said first, second and third lines are split in corresponding stages, each stage being separated through a corresponding repeater, the repeaters of the first and third lines being of the tristate type and being driven by the repeater of the second line when a congestion event occurs at the receiver block so that the data signal and the synchro signal are stored in the stages of the first and third lines." The Examiner concedes that Hirose fails to teach splitting the lines into stages. However, the Examiner points to Figure 1 of Applicants' specification and asserts that it would have been obvious to split. Applicants respectfully disagree.

It will be noted that Applicants' Figure 1 illustrates splitting the data and congestion lines into stages. Neither Hirose nor Applicants' Figure 1 teach having the synchro line split into stages. Furthermore, neither Hirose nor Applicants' Figure 1 teach connecting the data and congestion lines as claimed. The only teaching or suggestion for splitting the synchro line and connecting the data and congestion lines in the manner recited by claim 6 comes from Applicants' own disclosure (see, Figure 6). The Examiner is well aware of the prohibition against using hindsight from the Applicants' disclosure in making out a Section 103 rejection.

In view of the foregoing, allowance of claim 6 is requested. Claims 9 and 19 are asserted to be patentable over Hirose and the admitted prior art for at least the same reasons as claim 6.

Claim 11 was rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Farjad-rad. Claim 11 includes a limitation for having each "elementary block is realized through a multiplexer 2x2." These elementary blocks are "separated through a repeater." There is no teaching or suggestion in Farjad-rad for using the 2x2 circuit in a multiple form as a "communication network comprising a plurality of signal lines each split in elementary blocks." Still further, there is no teaching in Farjad-rad for having 2x2 circuits forming a signal line which are separated by repeaters. This configuration is likewise not taught or suggested by the Applicants' admitted prior art.

In view of the foregoing, allowance of claim 11 is requested.

Claim 12 was rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Farjad-rad and Hirose. This claim is patentable over the art of record for at least the reasons recited above with respect to claim 11. Additionally, Applicants point out that none of the cited prior art teachings address "negotiation to define the transmission direction" as claimed. As discussed above in connection with claim 8, the counters 18 and 18A of Hirose function to count stages (or commands) and thus ensure that there is not a transmission of more stages than the receiver can simultaneously process (see, col. 4, lines 15-64). This issue of trying to prevent congestion at the receiver has nothing to do with a "negotiation to define the transmission direction" as claimed. The Examiner's citation to Hirose fails to identify any manner with which Hirose functions to make a transmission direction negotiation

In view of the foregoing, allowance of claim 12 is requested.

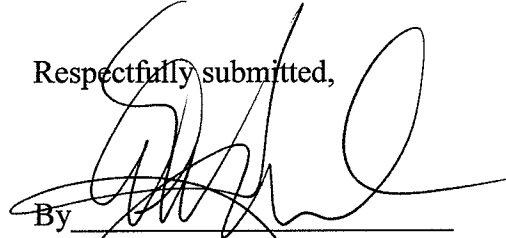
CUSTOMER NO. 32914

PATENT APPLICATION
Docket No. 61181-11USPX

Applicants respectfully submit that the application is now ready for allowance.

Dated: February 28, 2008

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'ASzuwalski', is written over a horizontal line. The signature is fluid and cursive.

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